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14. ABSTRACT

We observed that integrated low-dimensional structures on semiconductor detectors can steer a vertically oriented incident light-beams by almost 90 degrees, reduce surface reflection, slow down the light propagation velocity and increase photon-materials interactions. Such low-dimensional photon-trapping structures include nanoscale pillars, rods, holes, cones, funnels etc. Based on such observations, it is possible to design high speed photodetectors (PDs) with efficient light absorption capability while ensuring high speed performance in a number of materials. We designed and fabricated a CMOS compatible ultrafast surface illuminated silicon PD with 20 ps full width at half

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Report Title

Final Report: Heterogeneous Integrated Multispectral VIS-IR Sensors with Individually Addressable Spectrum

ABSTRACT

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Enter List of papers submitted or published that acknowledge ARO support from the start of the project to the date of this printing. List the papers, including journal references, in the following categories:

(a) Papers published in peer-reviewed journals (N/A for none)

Received		Paper
02/22/2017	9	Yang Gao, Hilal Cansizoglu, Kazim G. Polat, Soroush Ghandiparsi, Ahmet Kaya, Hasina H. Mamtaz, Ahmed S. Mayet, Yinan Wang, Xinzhi Zhang, Toshishige Yamada, Ekaterina Ponizovskaya Devine, Aly F. Elrefaie, Shih-Yuan Wang, M. Saif Islam. Photon Trapping Micro-/nanostructures Enable 2 High-Speed High Efficiency Silicon Photodiodes, Nature Photonics, ( ): . doi:
10/31/2016	2	Dewyani, Patil. A simple method to synthesize ?-Ga2O3 films for solar blindphotodetectors, IEEE Photonic Journal, (08 2015): 0. doi:
TOTAL:	**2**	

Number of Papers published in peer-reviewed journals:

(b) Papers published in non-peer-reviewed journals (N/A for none)

Received		Paper
TOTAL:		

Number of Papers published in non peer-reviewed journals:

(c) Presentations

Number of Presentations: 0.00

Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

Received	Paper
10/31/2016	5 HIlal, Cansizoglu. Efficient Si photovoltaic devices with integrated micro/nano holes, SPIE Nanoscience + Engineering. 29-AUG-16, San Diego, California, United States. : ,
10/31/2016	6 Ahmet, Kaya. Comparison of heterojunction device parameters for pure and doped ZnO thin films with IIIA (Al or In) elements grown on silicon at room ambient, SPIE Nanoscience + Engineering. 30-AUG-16, San Diego, California, United States. : ,
10/31/2016	7 Ahmet, Kaya. Ga2O3 as both gate dielectric and surface passivation via sol-gel method at room ambient, SPIE Optical Engineering + Applications. 30-AUG-16, San Diego, California, United States. : ,
10/31/2016	8 Ahmed S., Mayet. Inhibiting device degradation induced by surface damages during top-down fabrication of semiconductor devices with micro/nano-scale pillars and holes, SPIE Nanoscience + Engineering. 29-AUG-16, San Diego, California, United States. : ,
TOTAL:	**4**

Number of Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

Peer-Reviewed Conference Proceeding publications (other than abstracts):

Received	Paper
TOTAL:	

Number of Peer-Reviewed Conference Proceeding publications (other than abstracts):

(d) Manuscripts

Received	Paper
TOTAL:	

Number of Manuscripts:

Books

Received Book

TOTAL:

Received Book Chapter

TOTAL:

Patents Submitted

Patents Awarded

Awards

Graduate Students

NAME	PERCENT_SUPPORTED
FTE Equivalent:	
Total Number:	

Names of Post Doctorates

NAME	PERCENT_SUPPORTED
FTE Equivalent:	
Total Number:	

Names of Faculty Supported

NAME	PERCENT_SUPPORTED	National Academy Member
M.Saif Islam	0.11	Yes
FTE Equivalent:	**0.11**	
Total Number:	**1**	

Names of Under Graduate students supported

NAME	PERCENT_SUPPORTED
FTE Equivalent:	
Total Number:	

Student Metrics

This section only applies to graduating undergraduates supported by this agreement in this reporting period

The number of undergraduates funded by this agreement who graduated during this period: 0.00

The number of undergraduates funded by this agreement who graduated during this period with a degree in science, mathematics, engineering, or technology fields:..... 0.00

The number of undergraduates funded by your agreement who graduated during this period and will continue to pursue a graduate or Ph.D. degree in science, mathematics, engineering, or technology fields:..... 0.00

Number of graduating undergraduates who achieved a 3.5 GPA to 4.0 (4.0 max scale):..... 0.00

Number of graduating undergraduates funded by a DoD funded Center of Excellence grant for Education, Research and Engineering:..... 0.00

The number of undergraduates funded by your agreement who graduated during this period and intend to work for the Department of Defense 0.00

The number of undergraduates funded by your agreement who graduated during this period and will receive scholarships or fellowships for further studies in science, mathematics, engineering or technology fields:..... 0.00

Names of Personnel receiving masters degrees

NAME
Total Number:

Names of personnel receiving PHDs

NAME
Total Number:

Names of other research staff

NAME	PERCENT_SUPPORTED
FTE Equivalent:	
Total Number:	

Sub Contractors (DD882)

Inventions (DD882)

Scientific Progress

We observed that integrated low-dimensional structures on semiconductor detectors can steer a vertically oriented incident light-beams by almost 90 degrees, reduce surface reflection, slow down the light propagation velocity and increase photon-materials interactions. Such low-dimensional photon-trapping structures include nanoscale pillars, rods, holes, cones, funnels etc. Based on such observations, it is possible to design high speed photodetectors (PDs) with efficient light absorption capability while ensuring high speed performance in a number of materials. We designed and fabricated a CMOS compatible ultrafast surface-illuminated silicon PD with integrated nanoholes that exhibited 20-ps full-width at half-maximum (FWHM), and above 60% efficiency. The device is designed based on enhanced absorption in photon-trapping nano-structures integrated in a very thin PD that guarantees ultra-fast transit time for high speed operations. Our observations show pathways to convert indirect bandgap optical characteristic of silicon into material with direct bandgap optical properties by increasing the effective absorption coefficient or equivalently effective optical path for absorption by more than an order of magnitude.

Please see the manuscript under review by Nature Photonics

Technology Transfer

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Final Progress Report

Heterogeneously Integrated Multispectral VIS-IR Sensors with Individually Addressable Spectrum

ARO Grant # W911NF-14-4-0341

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Electrical and Computer Engineering Department
University of California, Davis

August 31, 2016

Summary: We fabricated photodetectors with integrated quasi-2D ridges and transfer-printed them onto secondary substrates. To achieve high quantum efficiency (QE) while keeping the detector thickness to the necessary minimum level required for transfer-printing, we attempted to employ 1D nano-pillars, nano-holes and 2D ridges for efficient photon trapping. We found that integrated nano-hole based devices are most attractive because they can be designed with a very thin absorption region and are easy to electrically interface without shielding the incoming photons. We also recognized that the proposed multispectral VIS-IR sensors with individually addressable spectrum is not feasible and useful for practical applications due to loss of resolution, mismatched lens for different spectrum and lack of appropriate read-out integrated circuitry (ROIC) with capability to offer individual addressability to four different materials on a single pixel. Based on these observations, a revised set of milestones is proposed for 12-24 months. We observed that integrated low-dimensional structures on semiconductor detectors can steer a vertically oriented incident light-beams by almost 90 degrees, reduce surface reflection, slow down the light propagation velocity and increase photon-materials interactions. Based on this observation, we designed and fabricated a CMOS compatible ultrafast surface-illuminated silicon PD with integrated nanoholes that exhibited 20-ps full-width at half-maximum (FWHM), and above 60% efficiency.

INTRODUCTION: Traditional IR photon detectors are designed with 2D epitaxial thin films that can occasionally involve low dimensional materials such as quantum dots (QDs) in the active regions. Multilayer antireflection (AR) coatings, surface texturing and innovative 3D pillar-like architectures contributed to enhanced efficiency and increased signal-to-noise ratio (SNR) via reduced dark current in devices enabled by reduced material volume. This resulted in increased temperature of operation compared to conventional IR detectors. During 2008-11, DOD sponsored PT-SQUAD teams conducted in-depth investigations on the potential of 3D pillars enabled photon trapping and enhanced photon absorption. This paved the way for the realization of wide spectral high-resolution infrared camera with high detectivity and low noise equivalent temperature using 3D-pillared pixels. However, a number of technical challenges remain to be addressed before the potentials of 3D textured detector materials can be practically used in IR systems. (***1***) First of all, can we electrically interface individual pillars with high performance contacts? (***2***) Can we spectrally resolve an image into a number of bands without penalties of increased size, weight and computational requirements? (***3***) What are the limitations associated with the spectral interrogation process? (***4***) Can we take advantage of already matured technology such as MEMS and high precision nanofabrication process for low-cost adaptive IR photon detection?

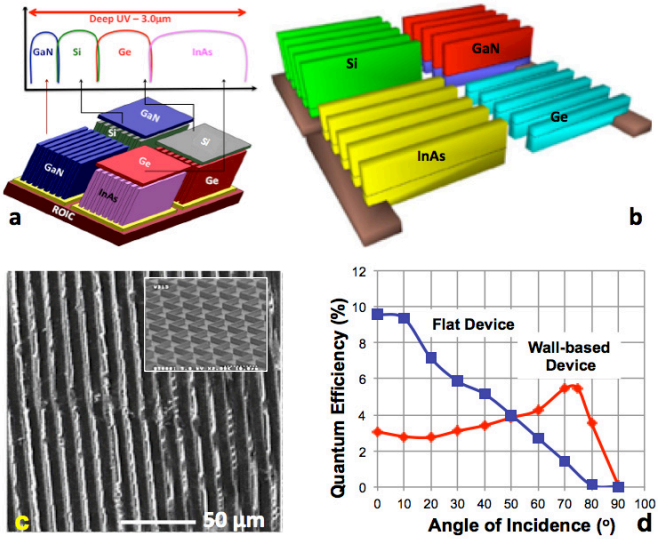

Figure 1. (a) Device structure that was proposed in the grant # ARO project # W911NF-14-4-0341. The focus was on the heterogeneous integration of multispectral VIS-IR sensors with individually addressable spectrum. (b) Schematic representation of different PD heights designed with different materials for optimum photo absorption. Such mismatch of heights, that vary between 2μm to 20μm, poses a great challenge when all these different materials need to be transfer-printed and electrically interfaced. (c) 2D wall shaped devices we fabricated and transfer-printed. The inset shows some zig-zag ridges designed to suppress polarization dependence. (d) Quantum-efficiency of transfer-printed wall-shaped devices at different photon incidence angles using white light (solar simulator) and comparison with devices with flat surfaces. Both devices didn't have AR coating or passivated surfaces. 70^{o} is optimal angle for 2D wall based devices and 0^{o} (perpendicular incidence) offers best efficiency in flat-top devices.

Key Observations and Challenges during ARO project # W911NF-14-4-0341: In last 2 years, we fabricated photodetectors with integrated quasi-2D ridges and transfer-printed them onto secondary substrates. Our goal was to fabricate photodetectors with photon-trapping capabilities using Si, Ge, GaN and InAs. As expected, the absorption depth of Si for optimum absorption is considerably higher than that of other materials. Transfer-printing of such materials with diverge heights and absorption coefficients is a considerable challenge. For example, more than 20μm high ridges are needed for high efficiency in Si detectors for 0.7μm to 1.0μm wavelengths, while less than 3μm Ge is sufficient for efficient detection for 1.0μm to 1.7μm wavelengths.

We also observed that proposed quasi-2D ridges exhibit *polarization dependence* and are not as effective as 1D pillars for high performance photon trapping. On the other hand, previously, when 1D-pillar shaped devices were used to design and transfer-print detectors, electrical interfacing of each pillars in a detector turned out to be a considerable challenge. Individual pillars need to be connected on both ends of the pillars. Metal contacts significantly attenuate light impacting device quantum efficiencies (QE). Although transparent conductors can be used to address this issue, most transparent conducting materials negatively impact the photon trapping properties. Based on these observations, we concluded that heterogeneously integrated multiple detectors on a single pixel with individually addressable connection may not be feasible and useful for practical applications.

Progress in Design of a Photoelectrochemical Etching System: It is well known that photoelectrochemical etching is a powerful tool for controlling the etching profile of microstructures. For example, the etching current of such a cell can be programmed in such a way that the resultant etching profile of a nanowire could have undulated features along the length of the wire. This may serve to increase photon trapping capabilities of the ensuing device compared to ordinary nanowire. As such, we felt that building up such a capability in our lab would offer us an additional avenue of pin pointing the most appropriate side wall morphology required to effect maximum photon collection. The design and fabrication of the photoelectrochemical etching system whose schematic is shown in Figure 2 below has been largely accomplished as listed below:

I. Fabrication of large electrochemical cell capable of handling 4 inch wafers
II. Fabrication of small electrochemical cell (handles test samples on less than 1 inch square)
III. Fabrication of a 500 watt LED arrays together with its cooling system.
IV. LabVIEW Interfacing of the power source that runs the cell and that which controls the lamp intensity

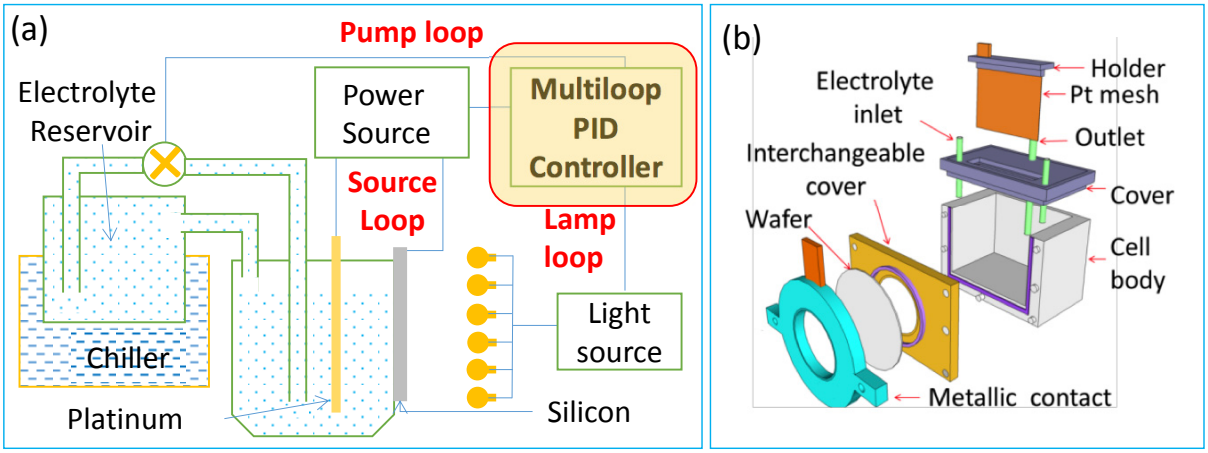

Figure 2 (a,b) A schematic of the photoelectrochemical etching system that includes an intercheable wafer holder. The light, chiller and power source are controlled by the multiloop PID controller as programed by a LabView Interface.

The schematic above epitomizes the layout of the etching system and indicates the key parts while scheme (b) illustrates the modular cell which can handle wafers from 2- 8 inches by using different interchangeable wafer holders.

Computer Interface for Etching Setup for Precise Control: The LabVIEW interfaces set up to coordinate the key instruments that make up the cell are set in such a way that a user friendly front panel allows the user to select an experiment to execute. Both static and dynamic current and potential processes can be executed with and without light. The major controls provided control: (i) Temperature of the cell by altering the speed at which the electrolyte is circulated between the chiller and the cell. (ii) Light intensity can be set independent or dependent on the cell's potential difference or current level. Allows for controls the hole generation available for reaction fluoride ion at the electrolyte/electrode interface. This controls the etching profile. A large number of holes favor isotropic etching while a lower number promotes anisotropicity. (iii) Cell potential and cell current control would allow for setting up the cell potential independent of the cell current and modulate the cell current with the light intensity. On the other hand setting up the cell current profile would be beneficial in the development of recipes for etching p-type wafers that do not need extra minority carriers (holes).

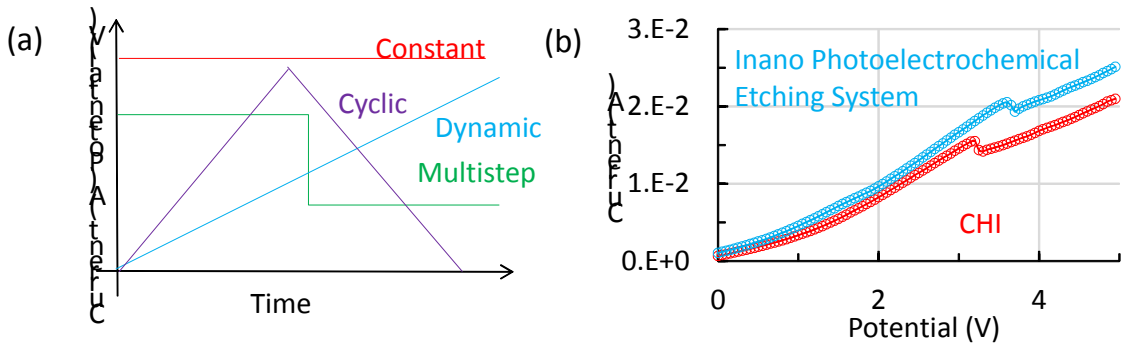

Figure 3. (a) A schematic of current and potential profiles that can be implemented on the developed photoelectrochemical cell. These profiles can be generated either independent of or dependent on the LED light. (b) A comparison of halve cyclic voltammogram of a *n*-type silicon wafer (1 Ωcm, 500µm thick) under strong illumination as ran by the inhouse developed etching system and controlled by the ensuing LabView interface (blue) in comparison to that controlled by the CH-Instrumes 660d potentiostat at a scan rate of 100mV/sec.

The developed LabVIEW can perform several experiments like an ordinary galvanostat or potentiostat. We have built interfaces to perform cyclic voltammetry, a key experiment in photoelectrochemical etching which defines potential and current levels that can promote either electro-polishing or hole formation during photoelectrochemical etching as shown in Figure 3 (b). We have benchmarked the half cyclic voltamogramm of an *n*-type silicon wafer (1 Ωcm, 500µm thick) from our cell and LabView interface with that obtained on the same cell controlled by the a state of the art CH-Instruments (CH-660D) potentiostat as shown in Figure 3b. The two half CVs are similar safe for the j_{ps} for the home built cell.

Preliminary Etching Results: 'V' grooves atop an *n*-type silicon wafer (1 Ωcm, 500µm thick) were generated using conventional photolithography and KOH etching techniques. As shown below and photoelectrochemical etching attempted at a current level of 20mA and a potential

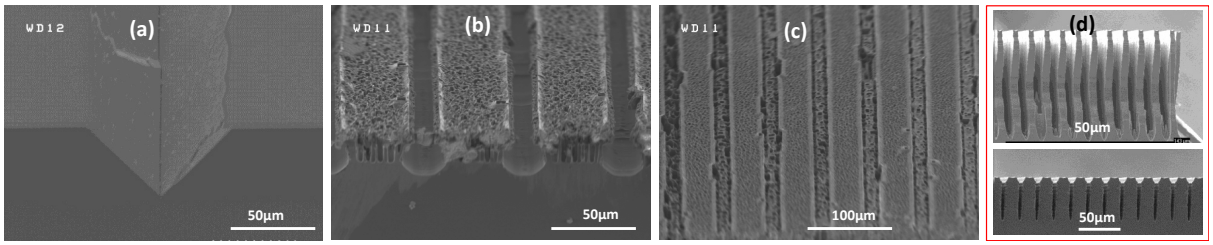

Figure 4. Cross-sectional micrograph of (a) KOH generated 'V' grooves atop a *n*-type silicon wafer (1 Ωcm, 500µm thick). (b) Upon photoelectrochemical etching at 3.0V for 0.5hr, 20mA current using our in built etching system (c) Upon photoelectrochemical etching at 3.5V for 0.5hr, 20mA. Notice that b and c exhibited. (d) Are the deep microwalls we had earlier obtained on which the 'V' grooves had been generated using a nitride mask.

difference of 3.5V (based on the CV shown in Figure 3). The SEM images in Figure 4 b and c indicate limited vertical etching of the wafers and a uniform distribution of the holes (30µm deep) that are randomly distributed on the entire surface of the wafer. Along the groove where anisotropic etching was expected, it was noted that a isotropic etching ensued while is some sections, uniform distribution of holes are noted.

The underlying problems unraveled: Based on the micrographs shown in Figure 4b-c, we conducted further experiments to establish possible reasons why anisotropic etching was unattainable even though characteristic cues on the CV had indicated that both isotropic and anisotropic photoelectrochemical etching was possible using the wafers we had. The CVs of the wafer as bought and after thermal oxide growth, photolithography patterning and KOH etching were obtained. Additionally, I-V curves of the wafer before and after generation of the 'v' grooves were obtained as shown in Figure 5 a and b.

We noted that after our wafer processing, the resistivity of the wafer increases significantly. As per now, we are not aware of the reason but we believe

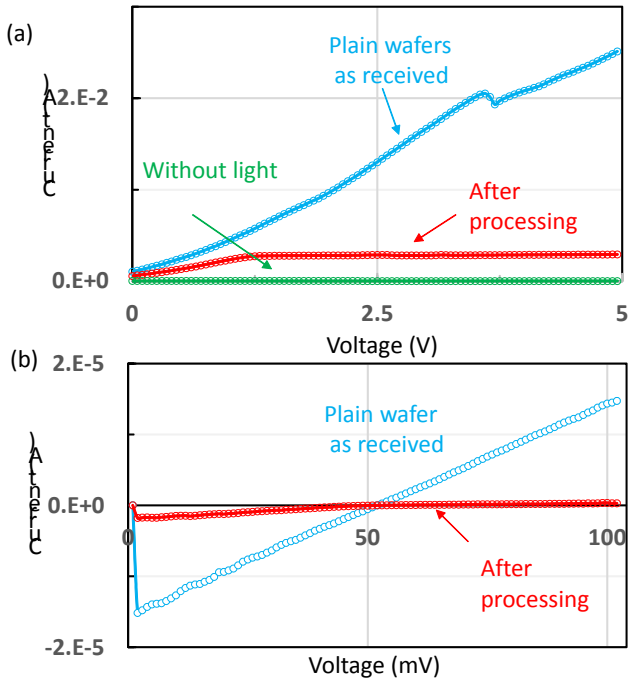

Figure 5. (a) Half CV of the wafer as received, after thermal oxidation and generation of 'V' grooves and removal of the masking oxide under high illumination and without illumination. Notice that there is a significant reduction in the current magnitude of the wafer after processing and it doe not exhibit the characteristic j_{ps} peak. The electrolyte used was 2.5% HF solution. (b) The I-V curve of the wafer before and after thermal oxidation processing indicating a signifant decrease in current magnitude of the latter, signifying an increase in overal wafer resistivity.

perhaps the high thermal oxidation process may be causing evaporation of the dopant ions.

Specific process modification modalities that we pursued:

(i) Processing the thermal oxide at a lower temperature to gauge whether it eliminates the increase in wafer resistivity after processing

(ii) Using a different oxide such as a nitride since our earlier experiments worked with 'V' grooves prepared using wafers having a nitride mask.

(iii) Instead of preparing grooves using KOH, micro trenches (< 100nm and 10μm deep) using DRIE. This eliminates the oxidation processes and ensures that the aspect ratio of the trenches allows for initiation of the anisotropic etching of the wafer at the trench bases.

Our Observations: The Proposed Deliverables of ARO project # W911NF-14-4-0341 was not Feasible and Useful for Practical Applications Due to the Following Reasons:

1. **Loss of Resolution**: Only 25% of the sensors are covered by devices made with each type of material, if each pixel of IR sensors is designed with four different materials (as shown in Figure 1a). This causes loss of resolution and much of the details are not be captured in an image.

2. **Lack of Appropriate Read-Out Integrated Circuitry (ROIC):** Commercially available ROICs are not designed to accommodate four different detectors in a single pixel with individual addressability. Even if four different detectors are transfer-printed on a single pixel, they are not be individually addressable.

3. **Mismatched Lens for Different Spectrum:** Even if different materials are transfer-printed to fabricate devices that cover a spectrum between 0.5μm to 3μm as was originally proposed, the field of view (FOV), lens focal length and modulation transfer function (MTF) are different for a wide spectrum of wavelengths. When detectors made of one material (such as Si) are activated while keeping others inactive to capture an image, the lens properties need to match the wavelengths of interest. As another group of detectors with a different material (such as InAs) are activated, the lens needs to be tuned to the new wavelengths of interest to generate high image quality. This poses an immense challenge, unless a manual lens changing protocol is adopted which defeats the purpose of having multiple integrated detectors with different materials for individually addressable spectrum.

4. **Uneven Detector Thickness:** Transfer-printing process is employed for integrating multiple detectors on a single substrate. This requires nearly equal vertical dimensions in each detector (same height in all the ridges). However, differences in absorption coefficients make each detector different in absorption length. In addition, challenges in growing thick epitaxial materials and etching such high aspect ratio ridges for most III-V semiconductors are great hurdles in implementing the proposed approach. Different thickness of the absorbing region makes it difficult to transfer-print different materials on to a single substrate.

5. **Unconventional Fabrication and Integration Challenges:** In order to separate four different spectra and reduce overlap of absorbed wavelengths, the design shown in Figure 1a presents a complex mechanism for shielding each kind of device from undesirable wavelengths. This includes covering the detectors with a thin film of wider bandgap material. For example, Si detectors can be covered with a GaN film and Ge detectors can be covered with a Si film. In addition to multiple interfaces that cause reflection/scattering loss, the integration process is a very cumbersome one. Furthermore, Si needs to be very thick to be an effective absorber of photons. All these contribute to a very difficult detector topology that cannot be processed easily. As was discussed before, designing detectors with pillars and ridges and their electrical interfacing always poses a great challenge.

Issues 1-3 cannot be addressed by using any known cost-effective technology. Issues 4-5 led us to develop approaches that contributed to highly efficient manufacturable detectors. Below we describe our observations and propose approaches to facilitate high performance electrical interfaces to detectors and spectrally resolve an image into a number of bands using a MEMS based external cavity enabled by high precision nano-fabrication process.

NEW FINDINGS: While trying to minimize the absorption thickness of Si to match it to that of Ge, GaN or InAs, we fabricated Si pin detectors with integrated holes for efficient photon trapping in a thinner absorbing region. We utilized deep UV stepper to define the dimensions of holes and pillars on the SOI substrates and etched the defined region with DRIE to be able to achieve successful fabrication of Si pin devices with integrated holes and pillars with precise dimensions.

Figure 6a shows the results of optical measurements obtained from two different structures of many Si pin detectors that we designed and fabricated so far. The reflectance of Si detector layers with integrated holes and pillars are compared with a planar Si detector. While Si with flat surface is reflecting ~25 % of light in the wavelength range of 500-900 nm, the reflectance from surfaces with pillars and holes is around ~ 15 % and ~5 %, respectively. That result suggests that integration of holes/pillars provide more efficient photon trapping compared to flat-top Si detectors. We believe that enhanced light trapping in the layer with holes/pillars results in higher absorption of light in the device layer. Note that in Figure 6a, the structure with holes has 64 % material loading whereas it's 36 % for the pillars (diameter of holes and pillars are 3µm with pitch length of 5 µm). The above results suggest that high amount of light can be absorbed by the device layer with integrated holes/pillars due to their efficient light trapping even if the structure has less amount of material loading. This surplus of devices with integrated

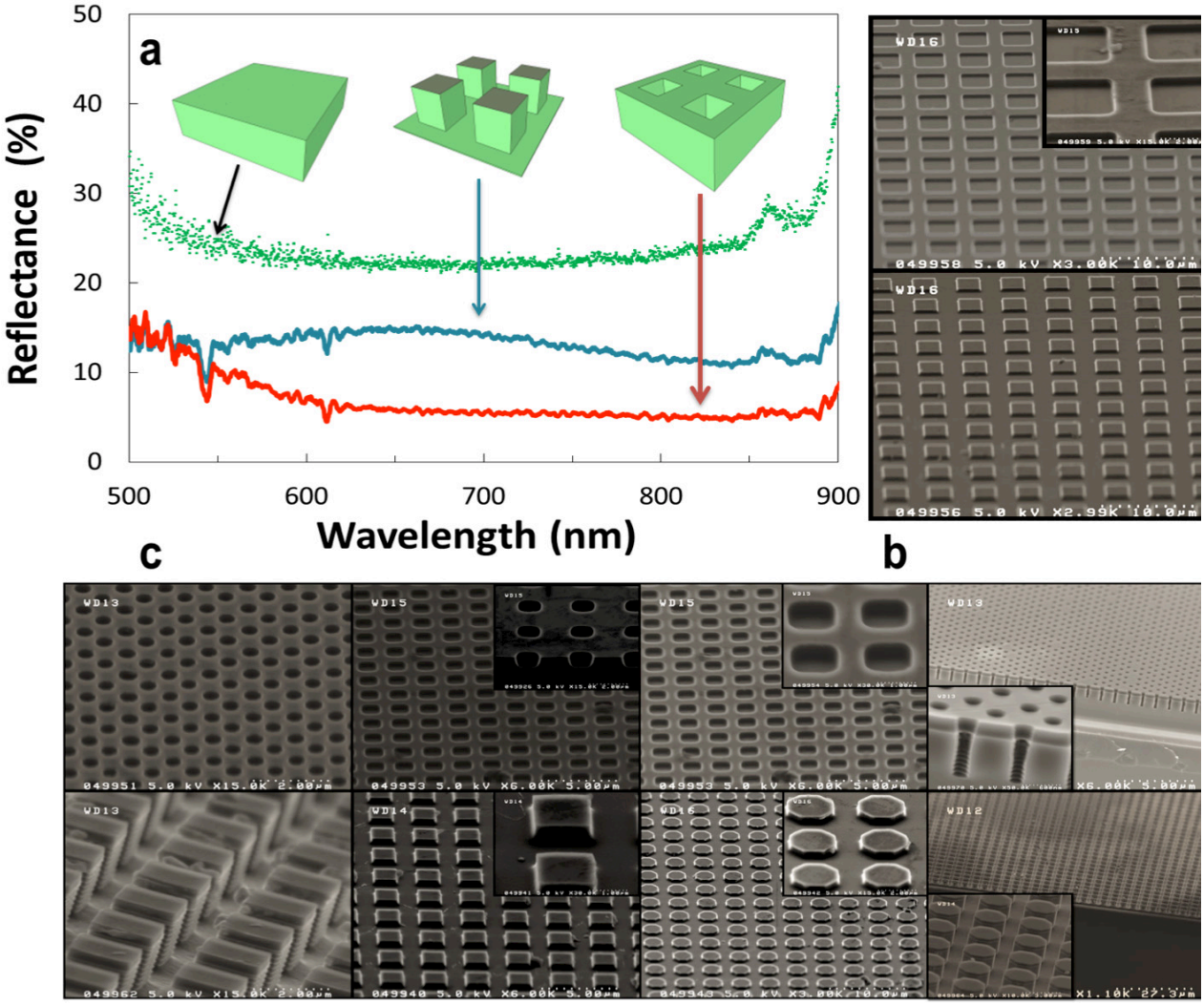

Figure 6. (a) Comparison of reflectance from Si pin detector with flat surface, pillars and holes. (b) Corresponding SEM images of the device layers with holes and pillars compared in (a). (c) SEM images of Si pin detectors with different design of holes and pillars.

holes/pillars can lead to fabricating detectors providing efficient light absorption along with suppressed dark current due to reduced material loading. Figure 6b shows the corresponding SEM images of those two structures compared in Figure 6a. As can be seen in Figure 6b, the device layer with integrated holes resembles a well-aligned network whereas the pillars are isolated from each other. The electrical interfacing of such an isolated structure is quite challenging. However, the device design with holes can provide an appropriate surface for planar metallization.

Combination of enhanced absorption of light with fewer amounts of material loading and ease on electrical interfacing makes the holes superior than the pillars in detection application. Figure 6c showcases SEM images of Si pin detectors that we fabricated successfully with integrated pillars and holes in various design and dimensions.

Figure 7a shows dramatically enhanced QE of such detectors. We designed these pin

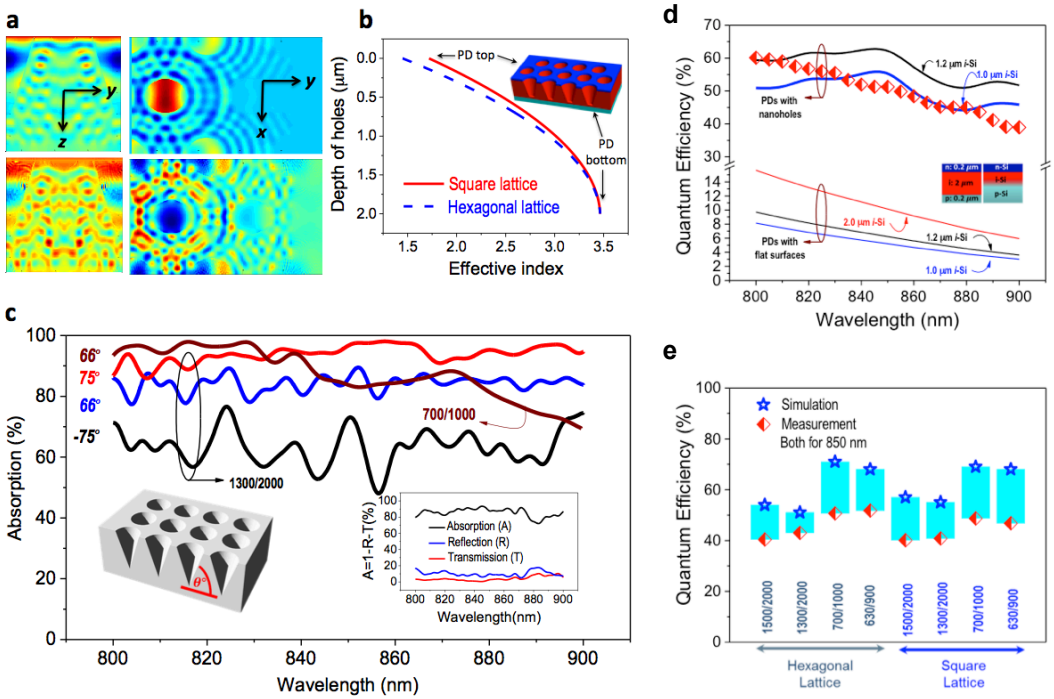

Figure 7. (a) Lateral field propagation in the in nanohole lattice: y-z plane in the left column and x-y plane in the right column. Time increases from top to bottom. For simulations, only left column of the holes was illuminated and the figure depicts the lateral wave propagating from left to right. (b) The effective refractive index vs distance from the top for the holes. The effective index profile gradually increases from the surface of the photodiodes to the bottom of the holes. c, Absorption (1-R-T) for holes with ~2 μm depth of etching in funnel shaped holes with angles of 75°, 66°, -75° (holes are wider at the bottom). The inset shows individual components; absorption (A), reflection (R) and transmission (T) for a cylindrical nanohole array. (d) Experimentally measured QE vs wavelengths for PDs with integrated nanoholes (red symbols). The measured QE was above 62 % at 800 nm and 52 % at 850 nm. The simulation results (black and blue lines at the top) show that our PDs with nanoholes have an absorbing i-Si layer thickness between 1.0 to 1.2 μm but absorbs as if we have more than 10μm Si. (e) Comparison of theoretical estimate (considering a 2 μm absorbing *i*-Si layer) and measured QE at 850 nm for PDs with nanoholes. The number at the bottom shows the hole diameter and periods.

devices with 2µm absorption layer having periodic etched holes on the surface. Highly enhanced QE (close to 60%) for 800nm was observed. Devices without holes (flat-top devices) exhibit ~10% QE for this wavelength. We developed a post-RIE etching process for surface damage removal and a rapid thermal annealing (RTA) step to mitigate the surface recombination issues. We show that these processes can effectively recover the carrier lifetime and dark current–voltage characteristics of the nanohole PDs to resemble the planar counterpart fabricated without RIE damages.

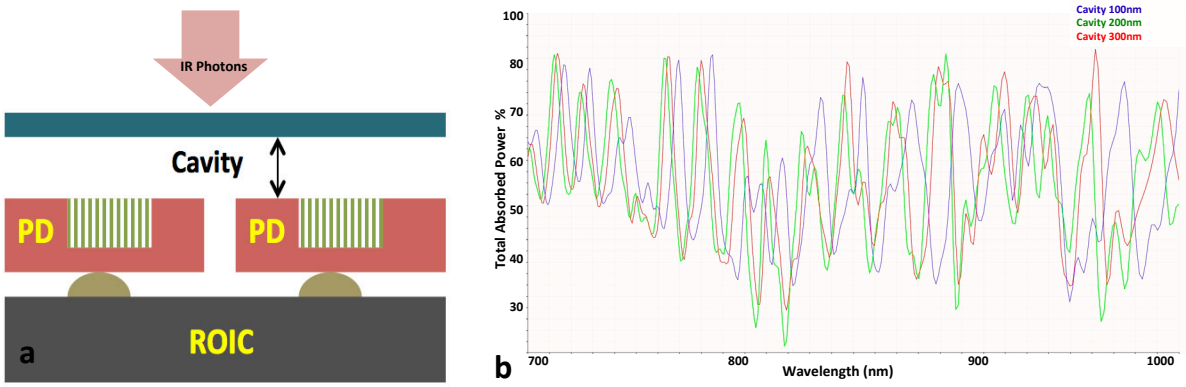

Figure 8. (a) Schematics of a thin-film based pin diode with periodic integrated photon trapping holes. Such devices exhibit close to an order of magnitude higher QE as shown in Figure 7a. Figure 7b shows the FDTD simulation of absorption, reflection and transmission for a detector QE with 2µm absorption layer. An external cavity can be integrated with this structure on the front side of the PD for tunable and spectrally resolved detection. (b) FDTD simulation (Lumerical Solutions, Inc.) data shows how detection peaks of the detectors can be tuned by tuning the external cavity length.

Detectors with Tunable External Cavity: We conducted detailed simulation of a structure (shown in the Figure 8a) that has a tunable external cavity integrated with hole-based pin detectors. Such a device shows potential for photon trapping with tunable and spectrally resolved detection capability without penalties of increased size and weight.

An external cavity can result in (**a**) a narrow spectral peak bandwidth, (**b**) high quantum efficiency (QE), and (**c**) low noise. Such detection peaks can be actively tuned over a broad wavelength region as shown in Figure 8b.

DOUBLE EXTERNAL TUNABLE CAVITY DETECTOR: A single cavity cannot effectively suppress undesirable wavelengths as shown in Figure 8b. Based on our preliminary simulation, we found that double cavity (a tunable Fabry-Perot etalon cavity inside another

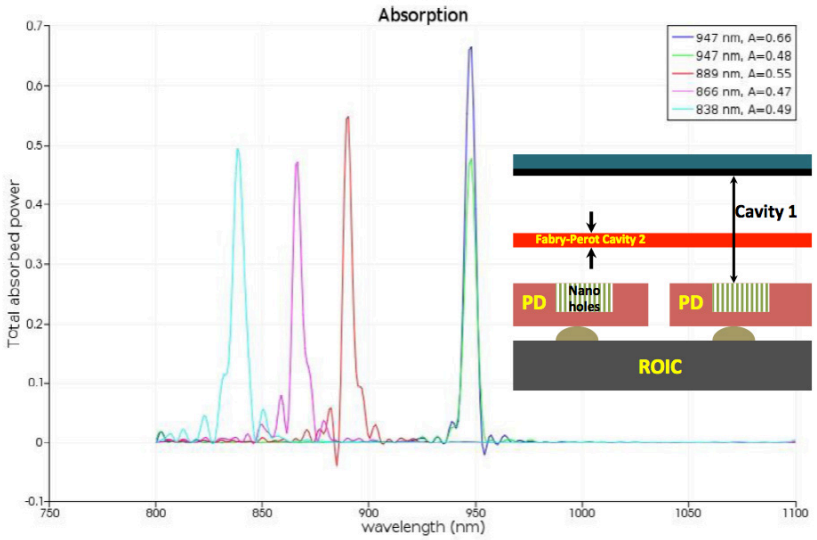

Figure 9. A double external tunable cavity integrated with hole-based detector. The structure offers wide wavelength tunability and high degree of unintended wavelength suppression. The absorption profile shown in Figure 3b can be modified with the applications of 2 tunable cavities.

tunable cavity) offers wide wavelength tunability and high degree of unintended wavelength suppression. Figure 9 presents the absorption spectra of a double cavity tunable detector. Recent developments in MEMS technology can be tapped for large scale, low-cost fabrication of such detectors with extreme precision and accuracy. Our proposed resonant detector structure is simpler and more versatile than the well-developed resonant cavity enhanced (RCE) photodetectors with integrated Bragg reflectors. A known drawback of RCE detectors is that they cannot be tuned once fabrication is complete.

Advantage of Detectors with Thin Absorption Region: Based on our numerical simulations, hole based structures are found to facilitate efficient photon trapping while effectively addressing the electrical interfacing challenge. The reduced and adjustable thickness of the active region of such a device helps in making such detectors extremely fast due to short transit time. This opens an opportunity for designing Si based ultra-fast photodetectors for data/telecommunication and other scientific applications. Thin absorbing layer contributes to reduced dark current (I_d) and the presence of holes suppresses the dark current even more (due to

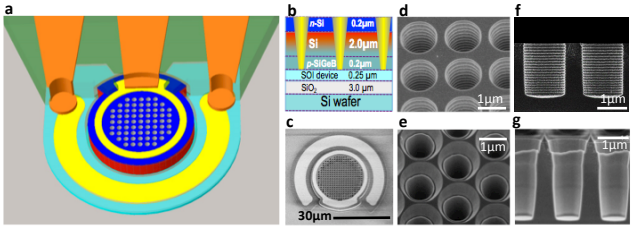

Figure 10. (**a**) Schematics of the ultrafast photodiode. (**b**) The *nip* PD structure on an SOI wafer showing the integrated tapered holes that span the *n, i* and *p*-layers. **c,** SEM micrograph of the active region of a high-speed PD with 30 μm diameter. (**d**) Square and (**e**) hexagonal hole lattice integrated in the PDs. Cross-section of (**f**), cylindrical and (**g**) funnel shaped or tapered holes etched into the active photodiode regions.

reduced material volume). We designed one such device (Figure 10) and demonstrated 20Gb/s data transmission capability in this device (Figure 11). We envision that more than 40GHz 3-dB bandwidth is attainable with such detectors designed with Si. Ultrafast Si detectors can contribute to reduced cost of optical received design for data centers, as well as telecom systems.

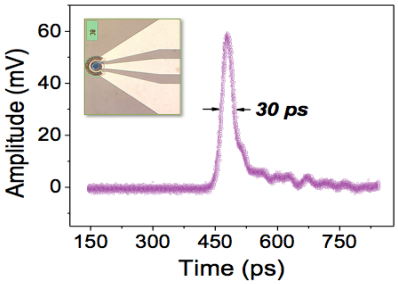

Figure 11. By illuminating a PD with a sub picosecond pulse, a 30 picosecond FWHM response was observed. When corrected for the oscilloscope bandwidth and laser pulse width, the device temporal response is estimated to be 20 ps at 850 nm. The inset shows an optical micrograph of a device with a high-speed coplanar waveguide (CPW) transmission line.

Key Achievements in 24 months:

1. We simulated and designed silicon (Si) detectors with integrated external tunable cavity that offers actively tunable detection peak over a broad wavelength region, as shown in Figure 8b. This was optimized for 0.7μm to 1.0μm wavelengths.
2. We simulated and designed integrated hole-based Ge pin photodetectors on Si substrate with tunable external cavity. We focused on optimizing wavelength between 1μm to 1.7μm.
3. Wet Etching Tool Development for Hole Etching: We developed electrochemical and photoelectrochemical etching methods for Si, Ge and HgCdTe to enable high aspect ratio etching of holes without causing surface damages that contribute to surface recombination and leakage currents.
4. We demonstrated a normal incident silicon photodiode with a impulse response of 20 picosecond FWHM, corresponding to a data transmission rate above 20 Gb/s or higher.
5. We designed a Ge counter part of a high-speed photodetector and are in the process of fabricating the device now.